

FIG. 1A

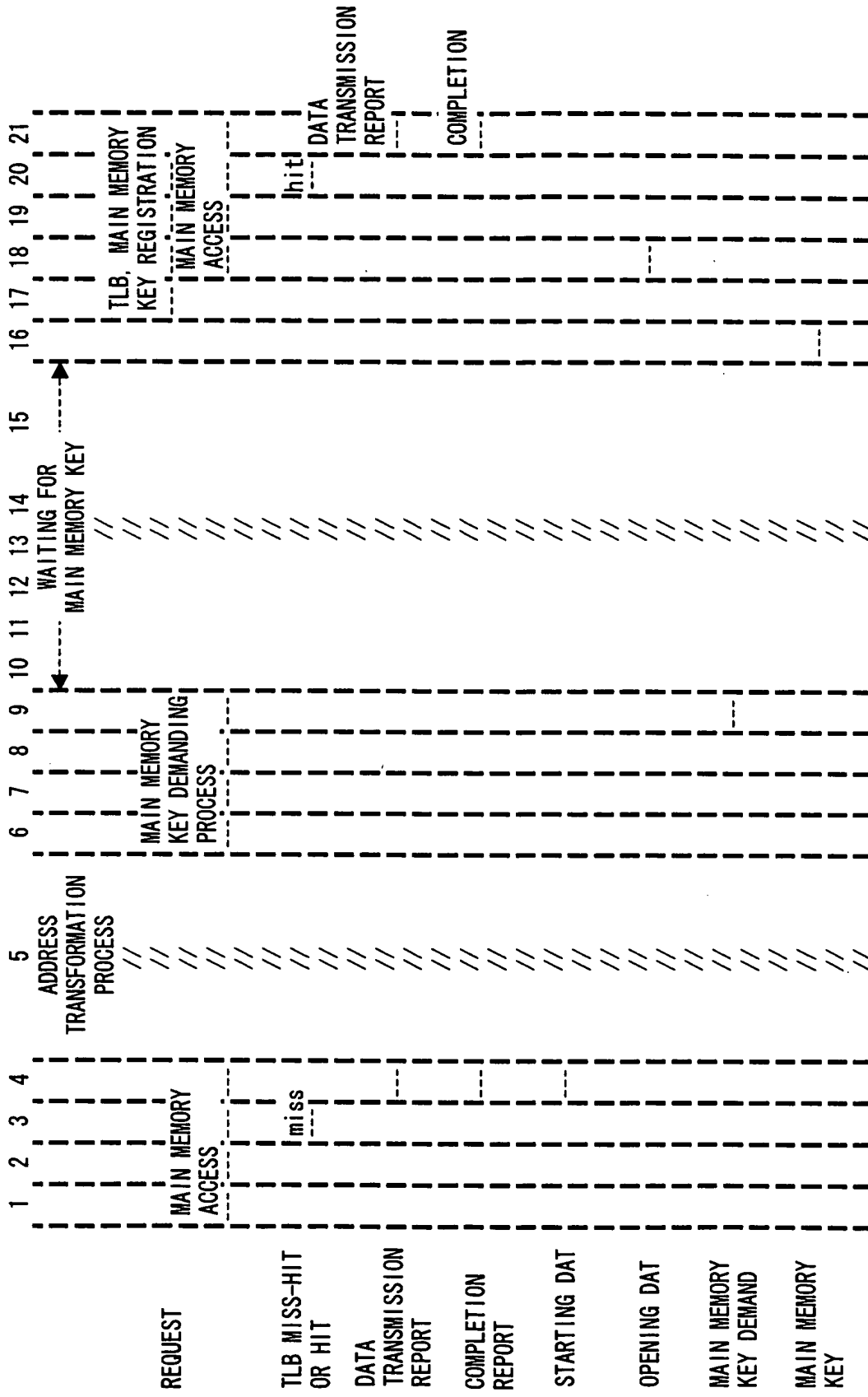


FIG. 1B

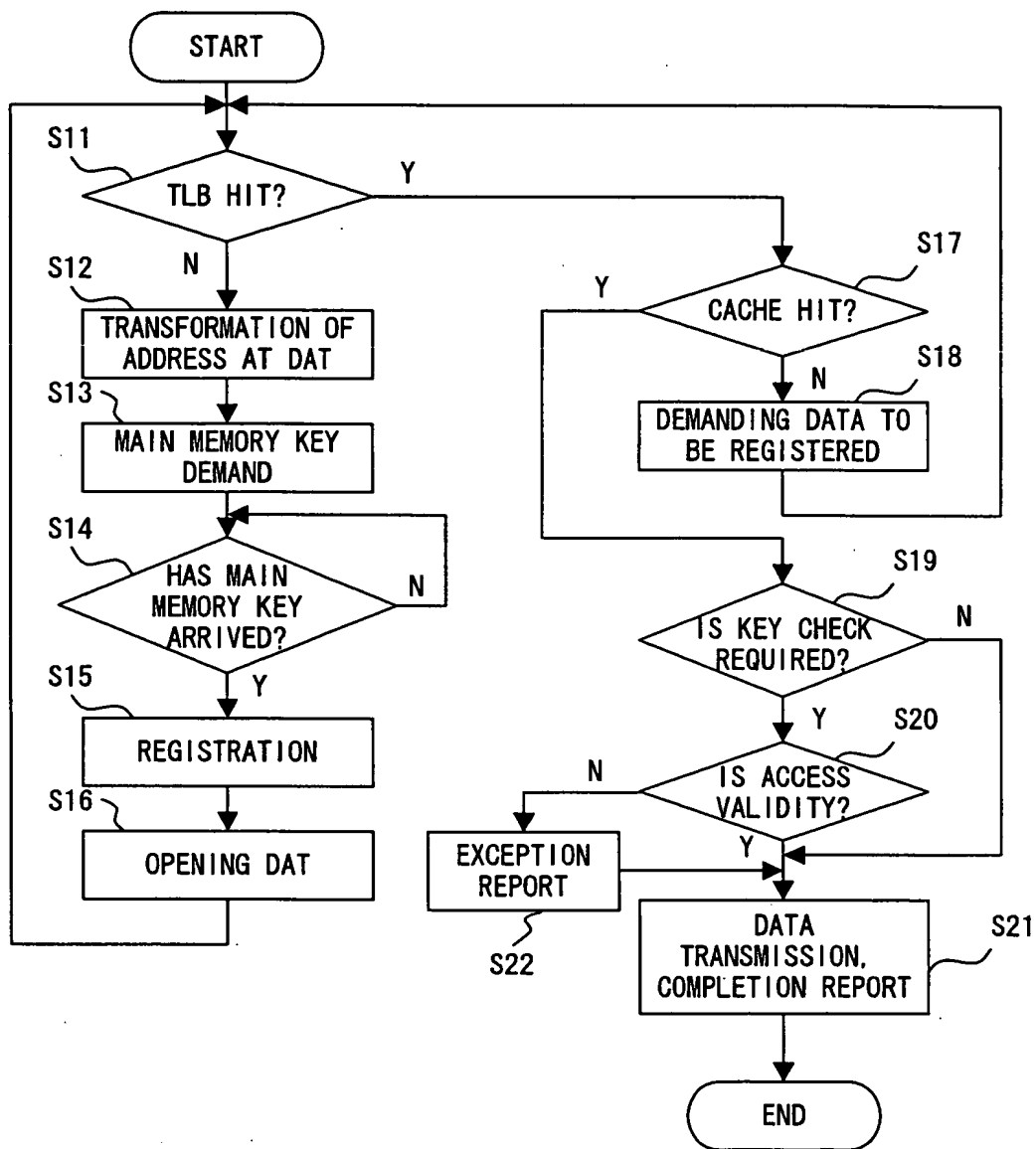


FIG. 1C

202301010001

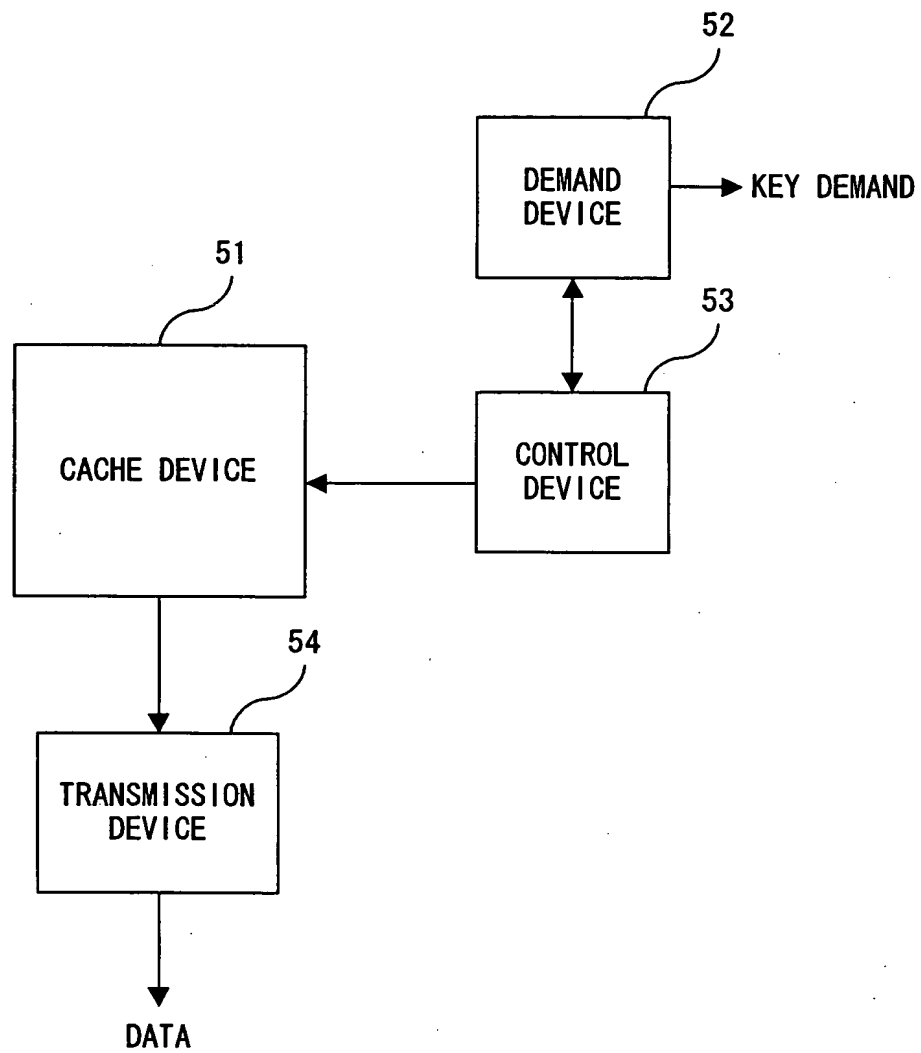


FIG. 2A

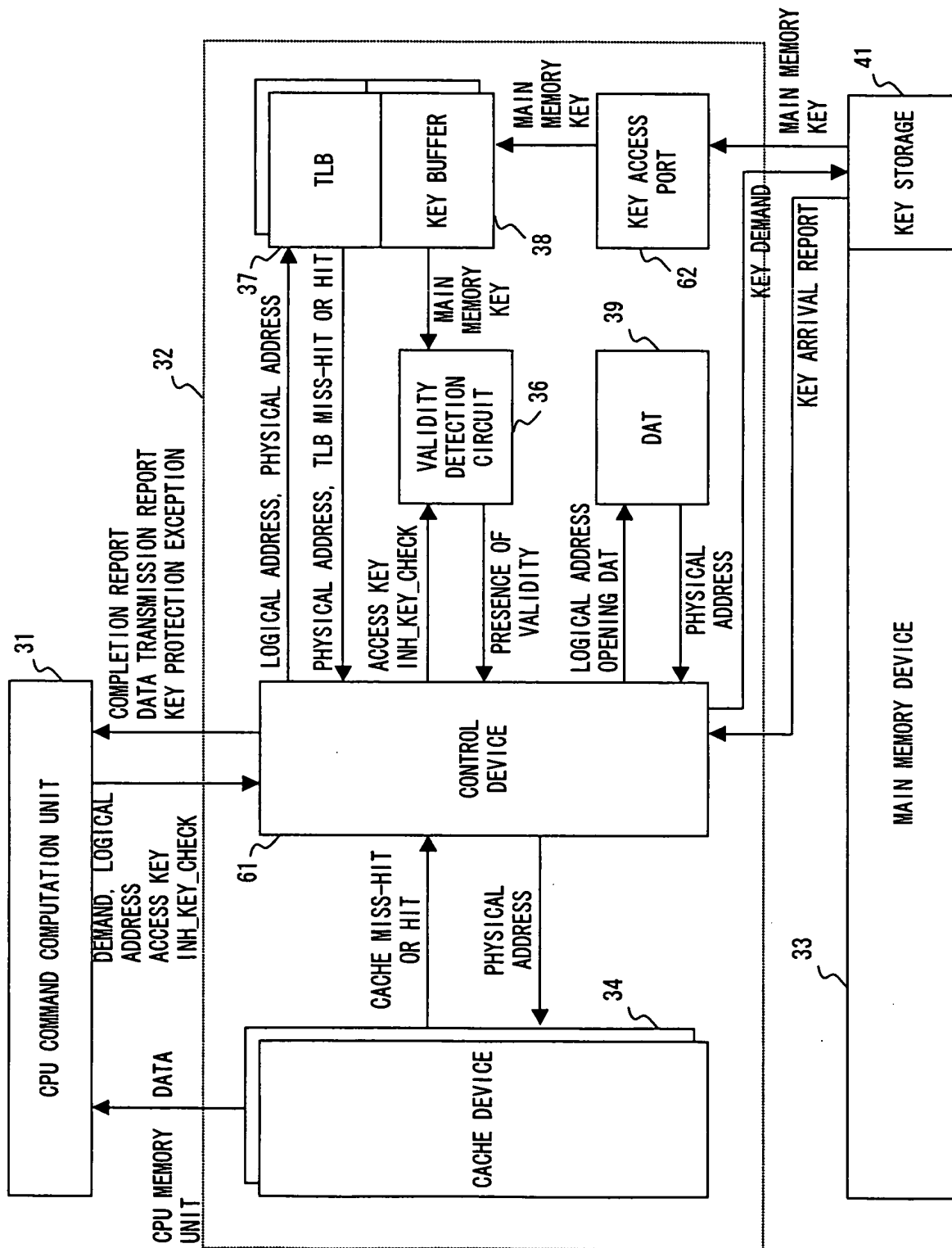


FIG. 2B

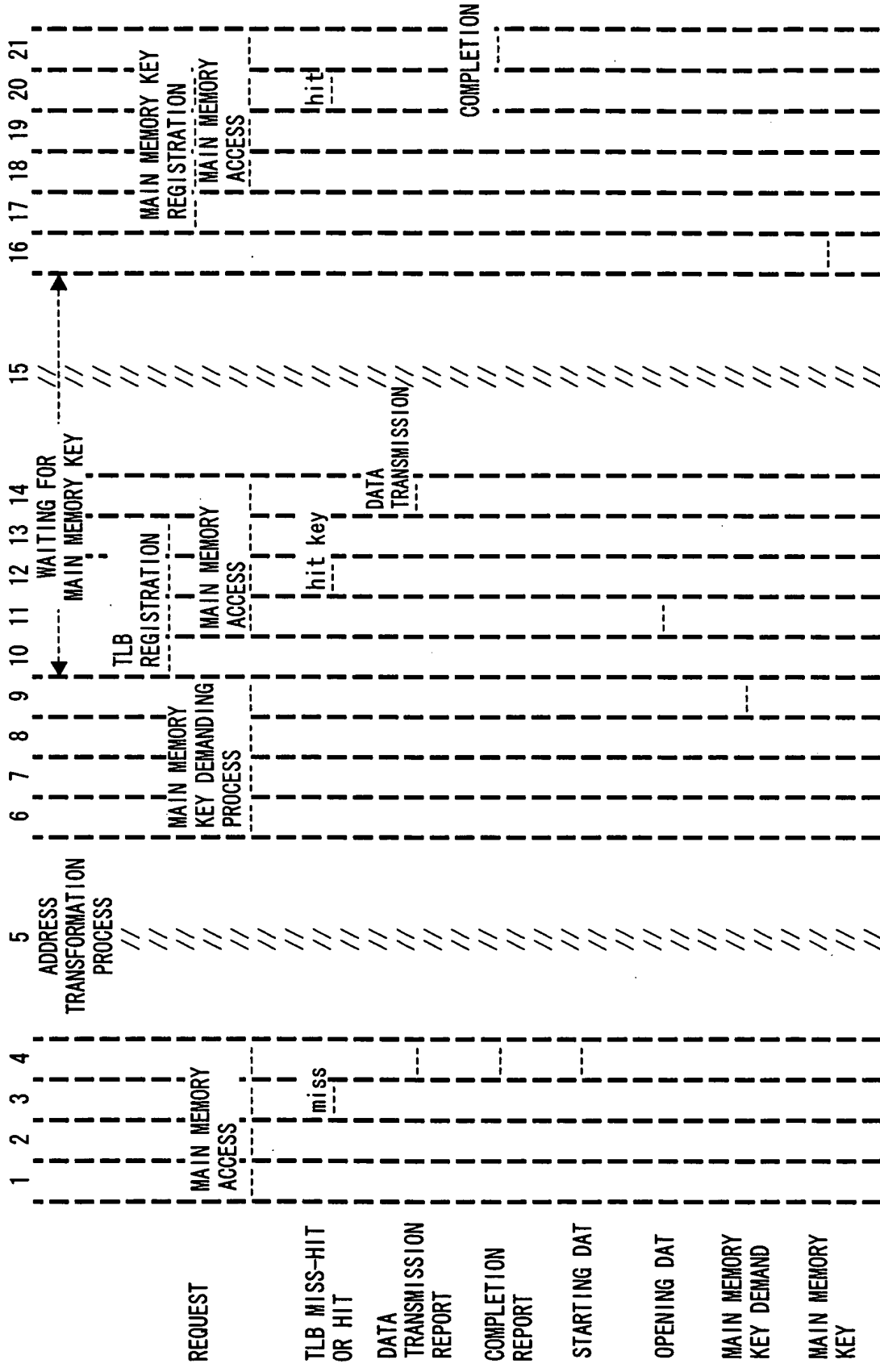


FIG. 3

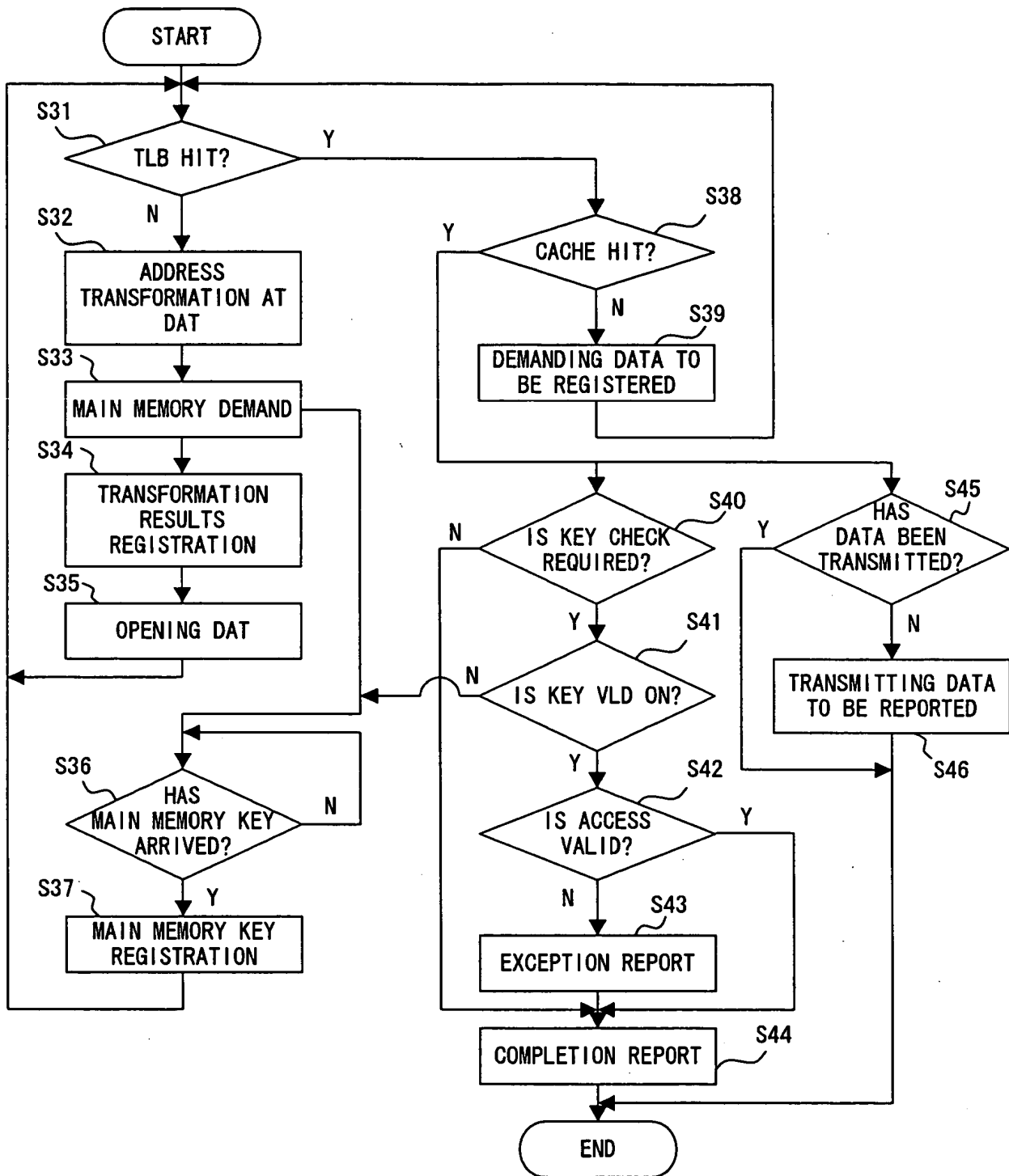


FIG. 5

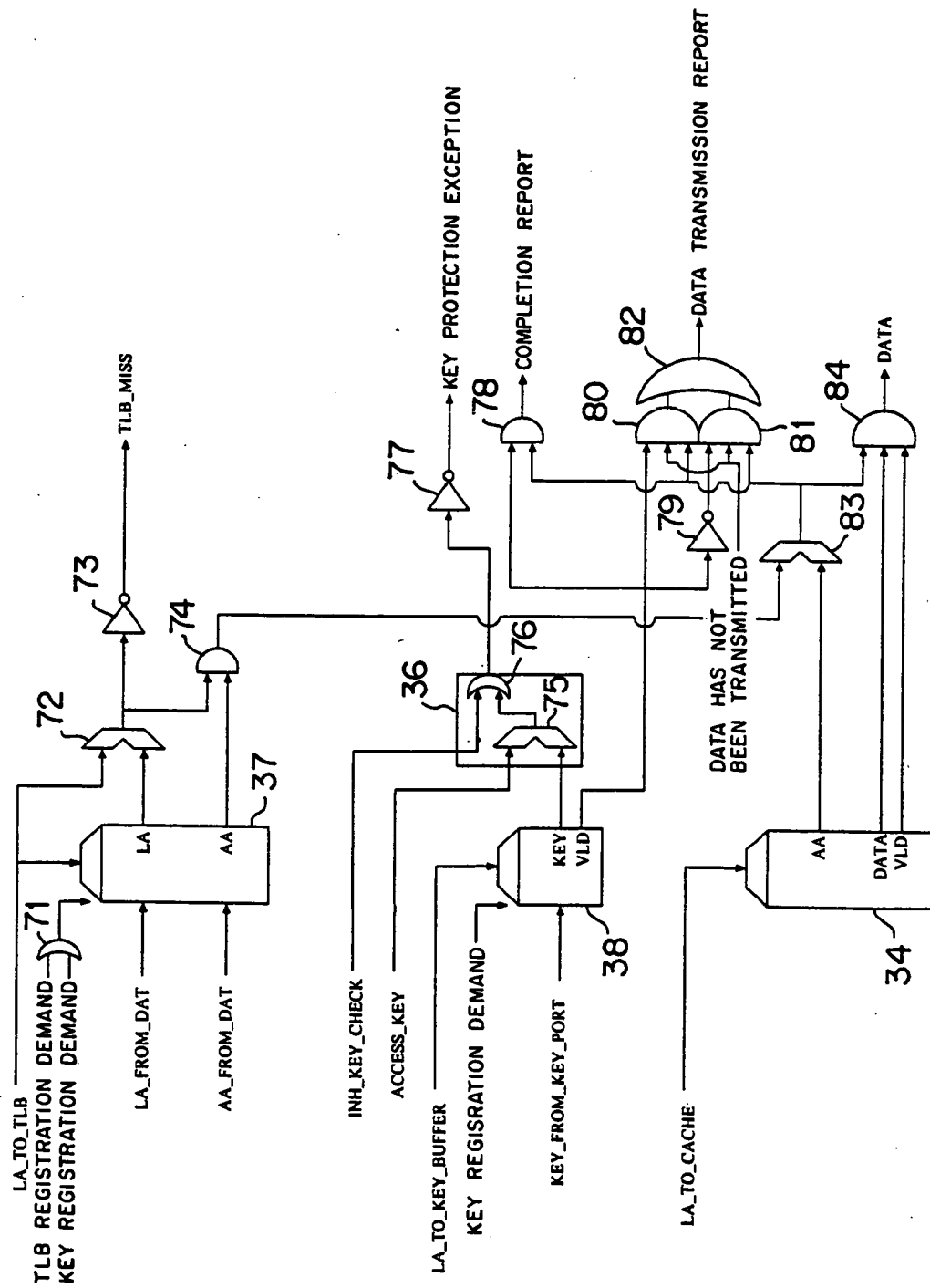


FIG. 6

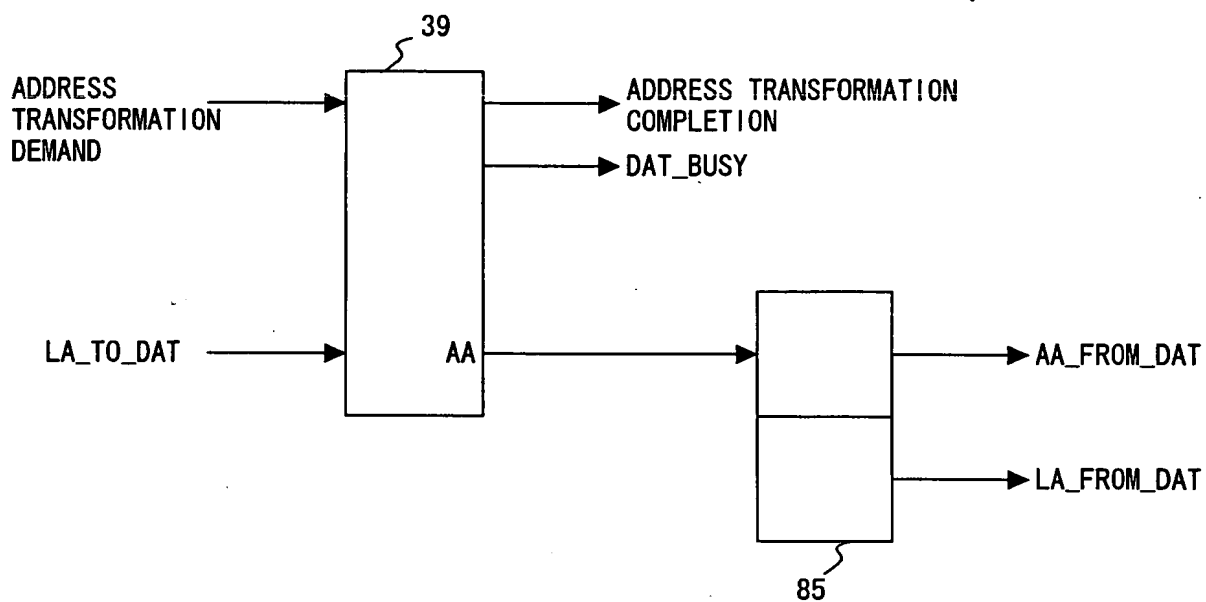


FIG. 7

20230101-191000

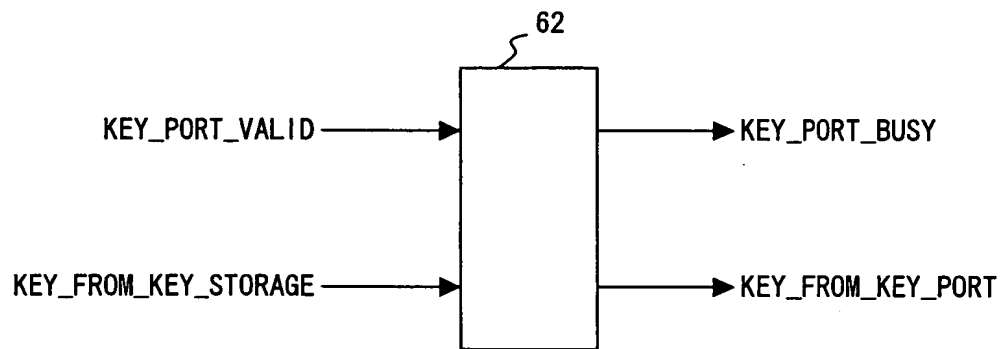


FIG. 8

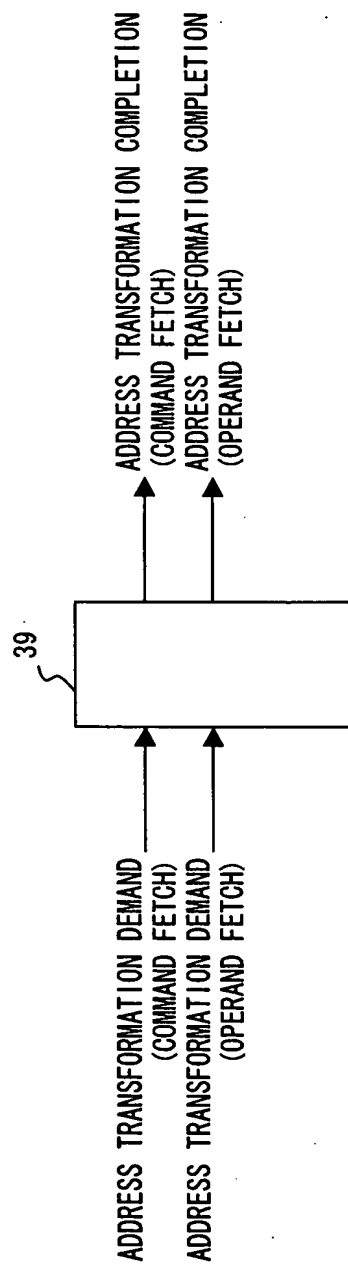


FIG. 10

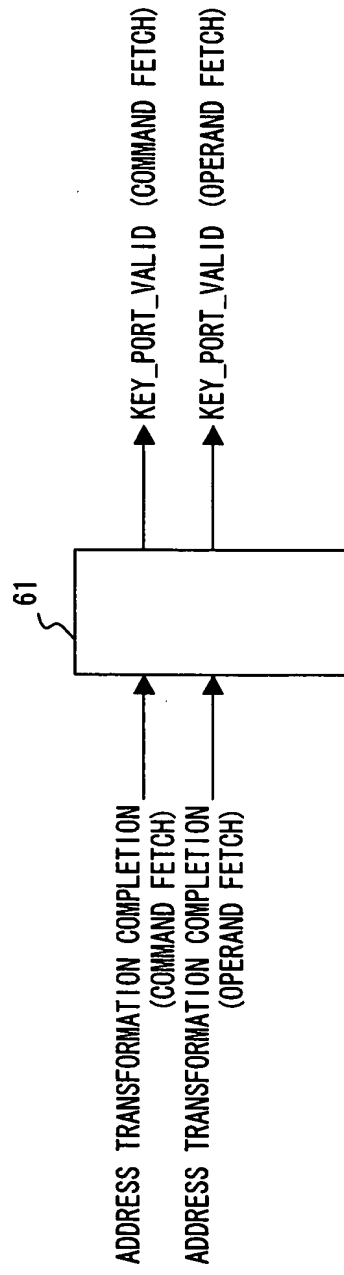


FIG. 11

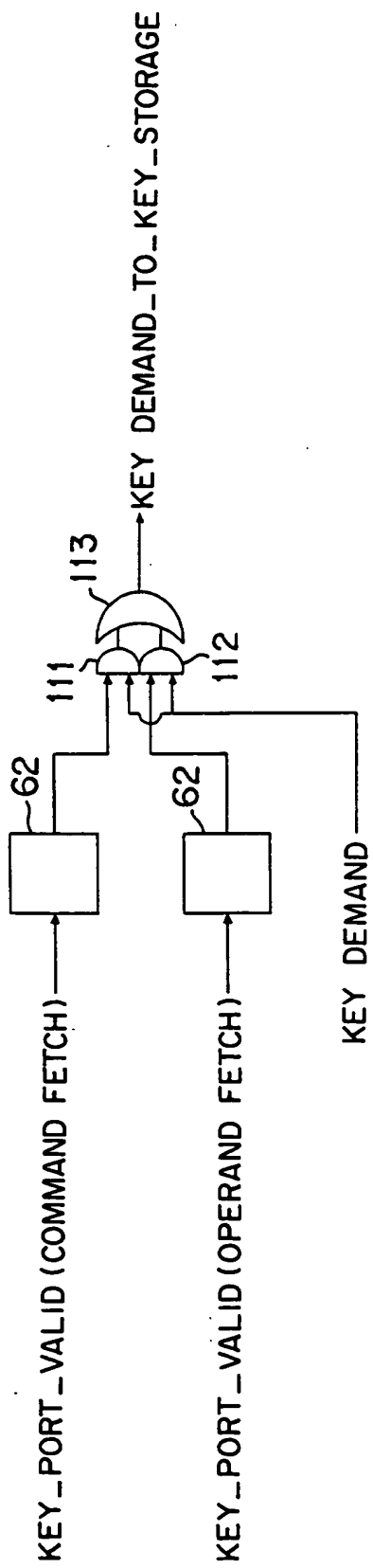


FIG. 12

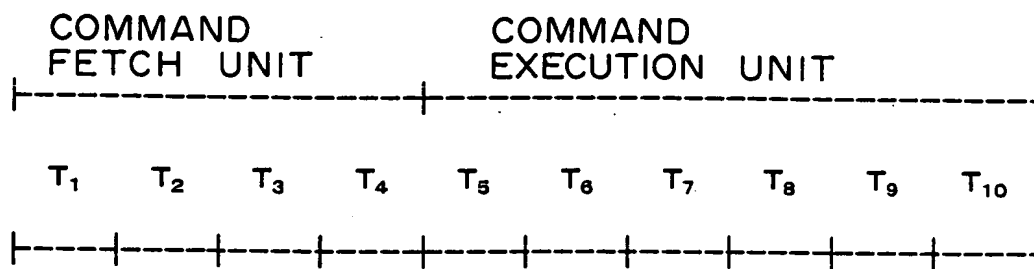
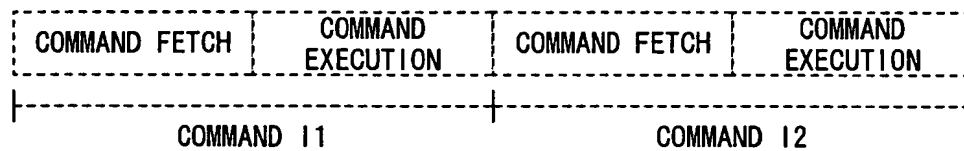


FIG. 13



F I G. 1 4

The diagram illustrates the timing of two commands, COMMAND 11 and COMMAND 12, relative to a common horizontal timeline. COMMAND 11 is represented by a dashed box divided into two sections: 'COMMAND FETCH' and 'COMMAND EXECUTION'. COMMAND 12 is represented by a similar dashed box, also divided into 'COMMAND FETCH' and 'COMMAND EXECUTION'. The 'COMMAND EXECUTION' phase of COMMAND 12 starts during the 'COMMAND EXECUTION' phase of COMMAND 11, showing that the processor can begin executing a new command before the previous one has fully completed its execution phase.

FIG. 15

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CONVENTIONAL



PRESENT INVENTION

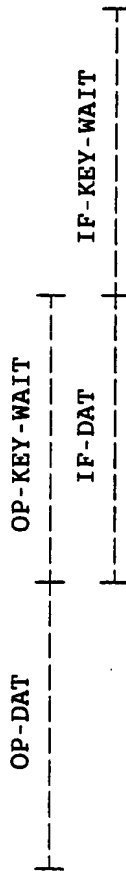
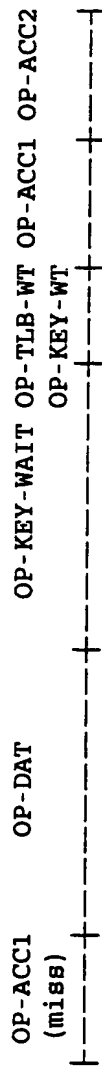


FIG. 16

CONVENTIONAL



PRESENT INVENTION

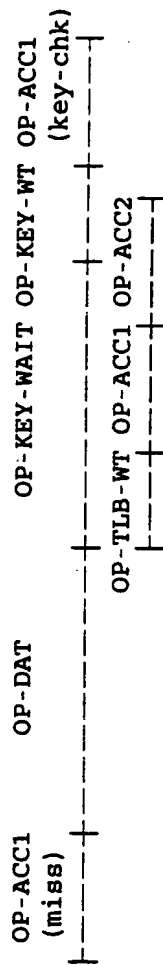


FIG. 17